Remarks

The non-final Office Action dated September 18, 2009, notes the following new grounds of rejection: claims 1 and 5-14 stand rejected under 35 U.S.C. § 103(a) over Thuringer (U.S. Patent No. 6,498,404) in view of Odinak (U.S. Patent No. 6,419,159); and claims 2-4 stand rejected under 35 U.S.C. § 103(a) over the '404 and '159 references in view of the Patterson reference ("Computer Architecture: A Quantitative Approach", pp. 134-135 1995). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 103(a) rejections of claims 1-14 because the proposed combination of the '404 and '159 references does not correspond to the claimed invention. Applicant respectfully submits that the rejections appear to be based primarily on the Office Action's misunderstanding of the operation of the cited embodiment of the '404 reference. In particular, the cited embodiment of the '404 reference does not teach separate current drawing and activity monitor circuits, with the current drawing circuit being controlled by the activity monitor circuit based on a combined activity signal derived by the activity monitor circuit as claimed. The Office Action continues to rely upon the load circuit discussed in Col. 1:28-38 of the '404 reference as allegedly corresponding to Applicant's current drawing circuit while failing to recognize that this load circuit is in fact the complementary gates (*e.g.,* AND gate 8 of Fig. 2) that are alleged to correspond to Applicant's activity monitor circuit. *See, e.g.,* Col. 1:45-52 and Col. 2:39-57. As such, the cited load circuit of the '404 reference does not correspond to Applicant's current drawing circuit. Applicant also notes that the complementary gates of the '404 reference function independently from one another and, as such, these complementary gates do not derive a combined activity signal indicative of a sum of power supply currents consumed by multiple processing circuits as does Applicant's activity monitor circuit.

Notwithstanding, to facilitate prosecution, Applicant has amended claims 1 and 7 to recite that each of the received pairs of processing signals includes input and output signals of one of the processing circuits. As is shown in Fig. 2 (*see also* Col. 1:45-65, and Col. 2:39-54), the AND gate 8 (*i.e.,* the asserted activity monitor circuit) does not

receive the output of the AND gate 5 (*i.e.,* the asserted processing circuit) and, as such, the relied upon embodiment of the '404 reference does not teach deriving activity information from the input and output signals of the processing circuits, as in the claimed invention. Applicant has further amended the claims to recite that the activity monitor circuit derives activity information, from each pair of processing signals, indicative of whether each of the processing circuits generates a logic level transition. Applicant submits that the cited portions of the '404 reference do not teach any such monitoring of a logic level transition of AND gate 5 (*i.e.,* the asserted processing circuit).

Turning now to the '159 reference, is appears that the Office Action acknowledges that the '404 reference does not teach an activity monitor circuit that derives a combined activity signal as claimed (*see* page 6 of the instant Office Action) and that the Office Action further asserts that such aspects are taught by the '159 reference. The '159 reference, however, does not teach any monitor circuit that monitors the device's normal power consumption. For example, the '159 reference does not teach monitoring the power consumed by portions of CPU 12 while it performs processing involving secret 20. *See, e.g.,* Fig. 1 and Col. 3:23-40. Instead, the '159 reference uses circuitry 40 to vary power fluctuations by using a random state generator 44 to randomly turn on and off some combination of current sinks while the processor 10 executes code. *See, e.g.,* Col. 3:35-55. In this regard, the '159 reference does not derive a combined activity signal indicative of the sum of power consumed by the processor 10 while it executes code.

In view of the above, the Office Action fails to cite to any reference that teaches or suggests various aspects of the claimed invention. Because neither reference teaches these aspects, no reasonable combination of these references can provide correspondence to the claimed invention. Accordingly, the § 103(a) rejections of claims 1-14 are improper and Applicant requests that they be withdrawn.

Applicant further traverses the § 103(a) rejections of claims 1-14 because the Examiner fails to provide a valid reason for the proposed combination of the '404 and '159 references, thus also failing to cite evidence of motivation for modifying the '404 reference. Consistent with M.P.E.P. § 2143.01 and relevant case law, a § 103 rejection must provide evidence of motivation where a proposed combination of references would modify a

primary reference. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that the skilled artisan would modify the '404 reference to include the random current drawing circuitry 40 of the '159 reference to "increase the security of the system by making the output power supply based on the randomness of the current sinks instead of making the output power supply constant as in (the '404 reference)." *See* page 7 of the instant Office Action. However, this hypothetical combination lacks any supporting evidence, and further does not provide a clearly-articulated reason that would be consistent with the *KSR* decision. In particular, the '404 reference teaches that it is the constant power consumption that disguises the actual power consumed by the data carrier during security-relevant operations. *See, e.g.,* Col. 1:45-65. The Office Action fails to present any evidence that the modification of the '404 reference would "increase the security of the system" relative to the unmodified '404 reference which already disguises the actual power consumed by the data carrier during security-relevant operations using complementary logic. As such, the Office Action's proposed modification involves adding redundant circuitry to the '404 reference without any perceived benefit.

Unlike the *KSR* decision, where the combination involved combining "two known devices according to their established functions", the Examiner's proposed combination does not involve simply combining teachings in which the cited references are not modified in their operation. More specifically, the proposed combination involves extensively modifying the '404 reference to somehow implement the random current drawing circuitry 40 of the '159 reference. Accordingly, the Examiner's assertion of such a vague "articulated reasoning" (*e.g.,* to "increase the security of the system") in support of the modification is insufficient. Particularly in view of the fact that the Office Action fails to present any evidence that the proposed combination would "increase the security of the system" relative to the unmodified '404 reference. *KSR* and M.P.E.P. § 2141 make it clear that such assertions are inapplicable where the operation of one of the references is modified. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007). For example, according to M.P.E.P. § 2141, Applicant can rebut such

assertions of obviousness simply by showing that "the elements in combination do not merely perform the function that each element performs separately." This is also consistent with various parts of *KSR*, which repeatedly refer to combined teachings in which the cited references are not modified in their operation. Accordingly, the § 103(a) rejections of claims 1-14 are improper and Applicant requests that they be withdrawn.

Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062.

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